Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1-76. (Canceled).

77. (Withdrawn) A method of making an integrated circuit comprising:

forming on a substrate circuitry including a plurality of integrated circuits having active devices; and

forming an elastic dielectric layer overlying the active devices;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

78. (Withdrawn) The method of claim 77, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

79. (Withdrawn) The method of claim 77 further comprising forming the elastic dielectric layer by deposition of one or more stress-controlled dielectric films.

80. (Withdrawn) The method of claim 79, wherein the one or more stress-controlled dielectric films are caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or

less and 2 to 100 times less than the fracture stress of the one or more stress-controlled dielectric films.

81. (Withdrawn) The method of claim 80, wherein the stress is tensile.

82. (Withdrawn) The method of claim 79 further comprising depositing at least one of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

83. (Withdrawn) The method of claim 77, wherein the substrate is at least one of a semiconductor substrate, a silicon substrate, and a dielectric substrate.

84. (Withdrawn) The method of claim 77 further comprising removing a major portion of the substrate.

85. (Withdrawn) The method of claim 84, wherein the integrated circuit is caused to be substantially flexible.

86. (Withdrawn) The method of claim 84, wherein the major portion of the substrate is removed prior to forming the circuitry.

87. (Withdrawn) The method of claim 84, wherein the major portion of the substrate is removed after forming the circuitry.

88. (Withdrawn) The method of claim 77 wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

89. (Withdrawn) The method of claim 88 wherein the integrated circuit is caused to be substantially flexible.

90. (Withdrawn) The method of claim 77, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

91. (Withdrawn) The method of claim 90, wherein the stress is tensile.

92. (Withdrawn) The method of claim 77, wherein the elastic dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

93. (Withdrawn) The method of claim 92, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

94. (Withdrawn) A method of making an integrated circuit, comprising:

forming on a substrate circuitry including a

plurality of integrated circuits having active devices;

forming an elastic dielectric layer overlying the active devices; and

removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

95. (Withdrawn) The method of claim 94, wherein the integrated circuit is caused to be substantially flexible.

96. (Withdrawn) The method of claim 94, wherein the major portion of the substrate is removed prior to forming the circuitry.

97. (Withdrawn) The method of claim 94, wherein the major portion of the substrate is removed after forming the circuitry.

98. (Withdrawn) The method of claim 94, further comprising forming the elastic dielectric layer by deposition of one or more stress-controlled dielectric films.

99. (Withdrawn) The method of claim 98, wherein the one or more stress-controlled dielectric films are caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the one or more stress-controlled dielectric films.

100. (Withdrawn) The method of claim 99, wherein the stress is tensile.

101. (Withdrawn) The method of claim 98 further comprising depositing at least one of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

102. (Withdrawn) The method of claim 94, wherein the substrate is at least one of a semiconductor substrate, a silicon substrate, and a dielectric substrate.

103. (Withdrawn) The method of claim 94, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

104. (Withdrawn) The method of claim 103, wherein the integrated circuit is caused to be substantially flexible.

105. (Withdrawn) The method of claim 94, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

106. (Withdrawn) The method of claim 105, wherein the stress is tensile.

107. (Withdrawn) The method of claim 94, wherein the elastic dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

108. (Withdrawn) The method of claim 107, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

109. (Currently Amended) A method of making an integrated circuit comprising:

forming a thin substrate; and

forming on the substrate circuitry including a plurality of integrated circuits having active devices~~, at least one of the integrated circuits having a uniform thickness throughout a full extent thereof~~;

wherein the integrated circuit is substantially flexible while retaining its structural integrity.

110. (Previously Presented) The method of claim 109, wherein the thin substrate is formed prior to forming said circuitry.

111. (Previously Presented) The method of claim 109, wherein the thin substrate is formed after forming said circuitry.

112. (Previously Presented) The method of claim 109 further comprising forming an elastic dielectric layer overlying the active devices.

113. (Previously Presented) The method of claim 112, further comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

114. (Previously Presented) The method of claim 113, further comprising depositing at least one of the elastic dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

115. (Previously Presented) The method of claim 112, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

116. (Previously Presented) The method of claim 115, wherein the stress is tensile stress.

117. (Previously Presented) The method of claim 112, wherein the elastic dielectric layer is formed from at least one of an inorganic and an organic dielectric material.

118. (Previously Presented) The method of claim 117, wherein the inorganic dielectric material is one of an

oxide of silicon, a nitride of silicon, silicon dioxide and silicon nitride.

119. (Previously Presented) The method of claim 109, wherein the substrate is at least one of a semiconductor substrate, a silicon substrate, and a dielectric substrate.

120. (Previously Presented) The method of claim 109, wherein said substrate is a dielectric.

121. (Previously Presented) The method of claim 109, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

122. (Currently Amended) A method of making an integrated circuit comprising:

forming a thin substrate;

forming on the substrate circuitry including a plurality of integrated circuits having active devices~~, at least one of the integrated circuits having a uniform thickness throughout a full extent thereof~~; and

wherein the integrated circuit is elastic while retaining its structural integrity.

123. (Previously Presented) The method of claim 122, wherein the thin substrate is formed prior to forming said circuitry.

124. (Previously Presented) The method of claim 122, wherein the thin substrate is formed after forming said circuitry.

125. (Previously Presented) The method of claim 122 further comprising forming an elastic dielectric layer overlying the active devices.

126. (Previously Presented) The method of claim 125, further comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

127. (Previously Presented) The method of claim 126, further comprising depositing at least one of the elastic dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

128. (Previously Presented) The method of claim 125, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

129. (Previously Presented) The method of claim 128, wherein the stress is tensile stress.

130. (Previously Presented) The method of claim 125, wherein the elastic dielectric layer is formed from at least one of an inorganic and an organic dielectric material.

131. (Previously Presented) The method of claim 130, wherein the inorganic dielectric material is one of an oxide of silicon, a nitride of silicon, silicon dioxide and silicon nitride.

132. (Previously Presented) The method of claim 122, wherein the substrate is at least one of a semiconductor substrate, a silicon substrate, and a dielectric substrate.

133. (Previously Presented) The method of claim 122, wherein said substrate is a dielectric.

134. (Previously Presented) The method of claim 122, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

135. (Currently Amended) A method of making an integrated circuit comprising:

forming a thin substrate; and

forming on the substrate circuitry including a plurality of integrated circuits having active devices~~, at least one of the integrated circuits having a uniform thickness throughout a full extent thereof~~;

wherein the integrated circuit is substantially flexible and elastic while retaining its structural integrity.

136. (Previously Presented) The method of claim 135, wherein the thin substrate is formed prior to forming said circuitry.

137. (Previously Presented) The method of claim 135, wherein the thin substrate is formed after forming said circuitry.

138. (Previously Presented) The method of claim 135 further comprising forming an elastic dielectric layer overlying the active devices.

139. (Previously Presented) The method of claim 138, further comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

140. (Previously Presented) The method of claim 139, further comprising depositing at least one of the elastic dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

141. (Previously Presented) The method of claim 138, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

142. (Previously Presented) The method of claim 141, wherein the stress is tensile stress.

143. (Previously Presented) The method of claim 138, wherein the elastic dielectric layer is formed from at least one of an inorganic and an organic dielectric material.

144. (Previously Presented) The method of claim 143, wherein the inorganic dielectric material is one of an oxide of silicon, a nitride of silicon, silicon dioxide and silicon nitride.

145. (Previously Presented) The method of claim 135, wherein the substrate is at least one of a semiconductor substrate, a silicon substrate, and a dielectric substrate.

146. (Previously Presented) The method of claim 135, wherein said substrate is a dielectric.

147. (Previously Presented) The method of claim 135, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

148. (Previously Presented) The method of claim 109 further comprising forming a stress-controlled dielectric layer overlying the active devices.

149. (Previously Presented) The method of claim 148 further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

150. (Previously Presented) The method of claim 149 further comprising depositing at least one of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

151. (Previously Presented) The method of claim 148, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

152. (Previously Presented) The method of claim 151, wherein the stress is tensile stress.

153. (Previously Presented) The method of claim 122 further comprising forming a stress-controlled dielectric layer overlying the active devices.

154. (Previously Presented) The method of claim 153 further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

155. (Previously Presented) The method of claim 154 further comprising depositing at least one of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

156. (Previously Presented) The method of claim 153, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

157. (Previously Presented) The method of claim 156, wherein the stress is tensile stress.

158. (Previously Presented) The method of claim 135 further comprising forming a stress-controlled dielectric layer overlying the active devices.

159. (Previously Presented) The method of claim 158 further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

160. (Previously Presented) The method of claim 159 further comprising depositing at least one of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

161. (Previously Presented) The method of claim 158, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

162. (Previously Presented) The method of claim 161, wherein the stress is tensile stress.

163. (Currently Amended) A method of making an integrated circuit comprising:

providing a thin substrate;

forming on the thin substrate circuitry having a plurality of active devices; and

wherein the integrated circuit is substantially flexible while retaining its structural integrity~~, and wherein the integrated circuit has a uniform thickness throughout a full extent thereof~~.

164. (Previously Presented) The method of claim 163 further comprising forming an elastic dielectric layer overlying the active devices.

165. (Previously Presented) The method of claim 164, further comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

166. (Previously Presented) The method of claim 165, further comprising depositing at least one of the elastic dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

167. (Previously Presented) The method of claim 164, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and

2 to 100 times less than the fracture strength of the elastic dielectric layer.

168. (Previously Presented) The method of claim 167, wherein the stress is tensile stress.

169. (Previously Presented) The method of claim 164, wherein the elastic dielectric layer is formed from at least one of an inorganic and an organic dielectric material.

170. (Previously Presented) The method of claim 169, wherein the inorganic dielectric material is one of an oxide of silicon, a nitride of silicon, silicon dioxide and silicon nitride.

171. (Previously Presented) The method of claim 163, wherein the substrate is at least one of a semiconductor substrate, a silicon substrate, and a dielectric substrate.

172. (Previously Presented) The method of claim 163, wherein said substrate is a dielectric.

173. (Previously Presented) The method of claim 163, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

174. (Previously Presented) The method of claim 163 further comprising forming a stress-controlled dielectric layer overlying the active devices.

175. (Previously Presented) The method of claim 174 further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

176. (Previously Presented) The method of claim 175 further comprising depositing at least one of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

177. (Previously Presented) The method of claim 174, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

178. (Previously Presented) The method of claim 177, wherein the stress is tensile stress.

179. (Currently Amended) A method of making an integrated circuit comprising:

providing a thin substrate;

forming on the thin substrate circuitry having a plurality of active devices; and

wherein the integrated circuit is elastic while retaining its structural integrity~~, and wherein the integrated circuit has a uniform thickness throughout a full extent thereof~~.

180. (Previously Presented) The method of claim 179 further comprising forming an elastic dielectric layer overlying the active devices.

181. (Previously Presented) The method of claim 180, further comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

182. (Previously Presented) The method of claim 181, further comprising depositing at least one of the elastic dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

183. (Previously Presented) The method of claim 180, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

184. (Previously Presented) The method of claim 183, wherein the stress is tensile stress.

185. (Previously Presented) The method of claim 180, wherein the elastic dielectric layer is formed from at least one of an inorganic and an organic dielectric material.

186. (Previously Presented) The method of claim 185, wherein the inorganic dielectric material is one of an

oxide of silicon, a nitride of silicon, silicon dioxide and silicon nitride.

187. (Previously Presented) The method of claim 179, wherein the substrate is at least one of a semiconductor substrate, a silicon substrate, and a dielectric substrate.

188. (Previously Presented) The method of claim 179, wherein said substrate is a dielectric.

189. (Previously Presented) The method of claim 179, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

190. (Previously Presented) The method of claim 179 further comprising forming a stress-controlled dielectric layer overlying the active devices.

191. (Previously Presented) The method of claim 190 further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

192. (Previously Presented) The method of claim 191 further comprising depositing at least one of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

193. (Previously Presented) The method of claim 190, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

194. (Previously Presented) The method of claim 193, wherein the stress is tensile stress.

195. (Currently Amended) A method of making an integrated circuit comprising:

providing a thin substrate;

forming on the thin substrate circuitry having a plurality of active devices; and

wherein the integrated circuit is substantially flexible and elastic while retaining its structural integrity~~, and wherein the integrated circuit has a uniform thickness throughout a full extent thereof~~.

196. (Previously Presented) The method of claim 195 further comprising forming an elastic dielectric layer overlying the active devices.

197. (Previously Presented) The method of claim 196, further comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

198. (Previously Presented) The method of claim 197, further comprising depositing at least one of the elastic dielectric films using at least one of multiple RF

energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

199. (Previously Presented) The method of claim 196, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

200. (Previously Presented) The method of claim 199, wherein the stress is tensile stress.

201. (Previously Presented) The method of claim 196, wherein the elastic dielectric layer is formed from at least one of an inorganic and an organic dielectric material.

202. (Previously Presented) The method of claim 201, wherein the inorganic dielectric material is one of an oxide of silicon, a nitride of silicon, silicon dioxide and silicon nitride.

203. (Previously Presented) The method of claim 195, wherein the substrate is at least one of a semiconductor substrate, a silicon substrate, and a dielectric substrate.

204. (Previously Presented) The method of claim 195, wherein said substrate is a dielectric.

205. (Previously Presented) The method of claim 195, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

206. (Previously Presented) The method of claim 195 further comprising forming a stress-controlled dielectric layer overlying the active devices.

207. (Previously Presented) The method of claim 206 further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

208. (Previously Presented) The method of claim 207 further comprising depositing at least one of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

209. (Previously Presented) The method of claim 206, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

210. (Previously Presented) The method of claim 209, wherein the stress is tensile stress.

211. (Withdrawn) The method of claim 77, further comprising forming a dielectric barrier layer in the

substrate before forming the active devices, wherein the dielectric barrier layer underlies the active devices.

212. (Withdrawn) The method of claim 77, wherein the elastic dielectric layer is caused to be substantially flexible.

213. (Withdrawn) The method of claim 77, further comprising forming a plurality of interconnect conductors within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

214. (Withdrawn) The method of claim 77, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

215. (Withdrawn) The method of claim 77, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

216. (Withdrawn) The method of claim 77, further comprising forming the elastic dielectric layer at a temperature of about 400°C.

217. (Withdrawn) The method of claim 94, further comprising forming a dielectric barrier layer in the

substrate before forming the active devices, wherein the dielectric barrier layer underlies the active devices.

218. (Withdrawn) The method of claim 94, wherein the elastic dielectric layer is caused to be substantially flexible.

219. (Withdrawn) The method of claim 94, further comprising forming a plurality of interconnect conductors within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

220. (Withdrawn) The method of claim 94, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

221. (Withdrawn) The method of claim 94, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

222. (Withdrawn) The method of claim 94, further comprising forming the elastic dielectric layer at a temperature of about 400°C.

223. (Previously Presented) The method of claim 109, further comprising forming a dielectric barrier layer underlying the active devices.

224. (Previously Presented) The method of claim 112, wherein the elastic dielectric layer is caused to be substantially flexible.

225. (Previously Presented) The method of claim 148, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

226. (Previously Presented) The method of claim 112, further comprising forming a plurality of interconnect conductors within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

227. (Previously Presented) The method of claim 112, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

228. (Previously Presented) The method of claim 112, further comprising forming the elastic dielectric layer at a temperature of about 400°C.

229. (Previously Presented) The method of claim 122, further comprising forming a dielectric barrier layer in the substrate before forming the active devices, wherein the dielectric barrier layer underlies the active devices.

230. (Previously Presented) The method of claim 125, wherein the elastic dielectric layer is caused to be substantially flexible.

231. (Previously Presented) The method of claim 153, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

232. (Previously Presented) The method of claim 125, further comprising forming a plurality of interconnect conductors within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

233. (Previously Presented) The method of claim 125, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

234. (Previously Presented) The method of claim 125, further comprising forming the elastic dielectric layer with a temperature of about 400°C.

235. (Previously Presented) The method of claim 135, further comprising forming a dielectric barrier layer in the substrate before forming the active devices, the dielectric barrier layer underlying the active devices.

236. (Previously Presented) The method of claim 138, wherein the elastic dielectric layer is caused to be substantially flexible.

237. (Previously Presented) The method of claim 158, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

238. (Previously Presented) The method of claim 138, further comprising forming a plurality of interconnect conductors within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

239. (Previously Presented) The method of claim 138, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

240. (Previously Presented) The method of claim 138, further comprising forming the elastic dielectric layer at a temperature of about 400°C.

241. (Previously Presented) The method of claim 163, further comprising forming a dielectric barrier layer in the substrate before forming the active devices, wherein the dielectric barrier layer underlies the active devices.

242. (Previously Presented) The method of claim 164, wherein the elastic dielectric layer is caused to be substantially flexible.

243. (Previously Presented) The method of claim 174, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

244. (Previously Presented) The method of claim 164, further comprising forming a plurality of interconnect conductors within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

245. (Previously Presented) The method of claim 164, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

246. (Previously Presented) The method of claim 164, further comprising forming the elastic dielectric layer at a temperature of about 400°C.

247. (Previously Presented) The method of claim 179, further comprising forming a dielectric barrier layer in the substrate before forming the active devices, wherein the dielectric barrier layer underlies the active devices.

248. (Previously Presented) The method of claim 180, wherein the elastic dielectric layer is caused to be substantially flexible.

249. (Previously Presented) The method of claim 190, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

250. (Previously Presented) The method of claim 180, further comprising forming a plurality of interconnect conductors within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

251. (Previously Presented) The method of claim 180, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

252. (Previously Presented) The method of claim 180, further comprising forming the elastic dielectric layer at a temperature of about 400°C.

253. (Previously Presented) The method of claim 196, wherein the elastic dielectric layer is caused to be substantially flexible.

254. (Previously Presented) The method of claim 206, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

255. (Previously Presented) The method of claim 195, further comprising forming a dielectric barrier layer underlying the active devices.

256. (Previously Presented) The method of claim 196, further comprising forming a plurality of interconnect conductors within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

257. (Previously Presented) The method of claim 196, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

258. (Previously Presented) The method of claim 196, further comprising forming the elastic dielectric layer at a temperature of about 400°C.

259. (Withdrawn) A method of making a circuit interconnect comprising:

forming on a substrate an elastic dielectric layer; and

forming a plurality of interconnect conductors within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors;

wherein the interconnect conductors are able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

260. (Withdrawn) The method of claim 259, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

261. (Withdrawn) The method of claim 260, wherein the stress is tensile.

262. (Withdrawn) The method of claim 259, wherein the elastic dielectric layer is caused to be substantially flexible.

263. (Withdrawn) The method of claim 259, further comprising depositing the elastic dielectric layer using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

264. (Withdrawn) The method of claim 259, wherein the wherein the substrate is at least one of a semiconductor substrate, a silicon substrate, and a dielectric substrate.

265. (Withdrawn) The method of claim 259, wherein the circuit interconnect is able to be thinned to about 50 microns or less while retaining its structural integrity.

266. (Withdrawn) The method of claim 259, further comprising removing a major portion of the substrate.

267. (Withdrawn) The method of claim 266, wherein the circuit interconnect is caused to be substantially flexible.

268. (Withdrawn) The method of claim 259, wherein the circuit interconnect is caused to have a thickness of about 50 microns or less.

269. (Withdrawn) The method of claim 268, wherein the circuit interconnect is caused to be substantially flexible.

270. (Withdrawn) The method of claim 259, wherein the circuit interconnect is capable of forming at least one of a substantially flexible circuit interconnect and an elastic circuit interconnect.

271. (Withdrawn) The method of claim 259, wherein the elastic dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

272. (Withdrawn) The method of claim 271, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.